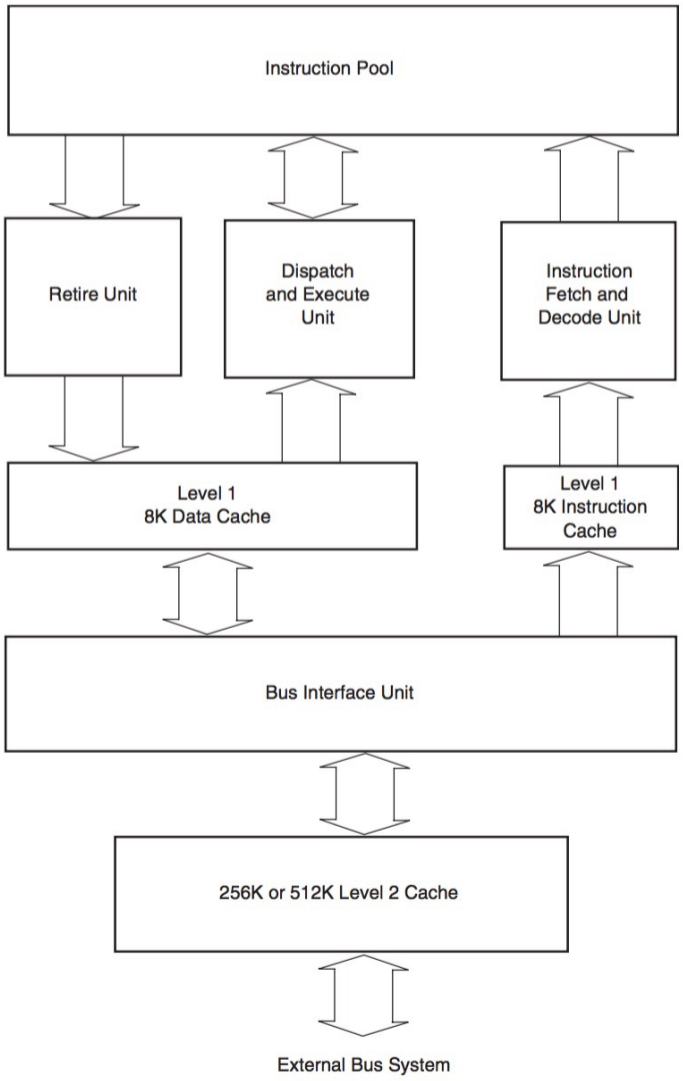
MP Assignment V

1.

A. With a neat diagram, explain the internal structure of Pentium Pro.



The Pentium Pro is structured differently than earlier microprocessors.

The system buses, which communicate to the memory and I/O, connect to an internal level 2 cache that is often on the main board in most other microprocessor systems. The level 2 cache in the Pentium Pro is either 256K bytes or 512K bytes.

The bus interface unit (BIU) controls the access to the system buses through the level 2 cache, which is integrated in Pentium Pro. The BIU generates the memory address and control signals, and passes and fetches data or instructions to either a level 1 data cache or a level 1 instruction cache.

The instruction cache is connected to the instruction fetch and decode unit (IFDU).

Pentium Pro can process two integer instructions and one floating-point instruction simultaneously.

The dispatch and execute unit (DEU) retrieves decoded instructions from the instruction pool when they are complete, and then executes them.

Pentium Pro has a RU (Retire unit) which checks the instruction pool and removes decoded instructions that have been executed.

B. List the new features added to Pentium Pro when compared with its predecessors with respect to memory system.

The memory system for the Pentium Pro microprocessor is 4G bytes in size, similar to 80386DX–Pentium microprocessors, but access to an area between 4G and 64G is made possible by additional address signals A_{32-35}.

In the Pentium Pro microprocessor, the bank enable signals (BE_{7-0}) are **multiplexed** on the address bus A_{15-8}, Address available during the first clock cycle and the bank enable during the second clock cycle of a memory or I/O access.

Pentium Pro has the capability to **check and generate parity for the address bus** during certain operations. The AP pins provide the system with parity information, and a bad parity check for the address bus.

There is built-in **error-correction circuit** (ECC) on the Pentium Pro that allows the *correction of a one-bit error* and the *detection of a two-bit error*.

2.

A. Explain in detail about the software changes in Pentium II when compared to Pentium Pro.

The Pentium II microprocessor core is a Pentium Pro. It is basically a more consumer-oriented version of the Pentium Pro. It was cheaper to manufacture because of the separate, slower L2 cache memory.

In a pentium II,

The SYSENTER and SYSEXIT instructions use the fast call facility introduced in the Pentium II microprocessor.

The SYSENTER instruction uses some of the model-specific registers to store CS, EIP, and ESP to execute a fast call to a procedure defined by the model-specific register.

The SYSEXIT instruction loads CS and SS with the selector pair addressed by SYSENTER_CS plus 16 and 24.

The FXSAVE instruction added in the Pentium II is designed to properly store the state of the MMX machine. The FSAVE instruction stores the entire tag field, whereas the FXSAVE instruction only stores the valid bits of the tag field. The valid tag field is used to reconstruct the restore tag field when the FXRSTOR instruction executes.

B. Discuss the following signals of Pentium Pro Processor:

A. LOCK

LOCK# becomes a logic 0 whenever an instruction is prefixed with the LOCK: prefix. This is most often used during DMA accesses.

B. D_{63} - D_0

Data bus connections transfer byte, word, double-word, and quadword data between the microprocessor and its memory and I/O system.

C. AP_1# - AP_0#

Address parity provides even parity for the memory address on all Pentium Pro–initiated memory and I/O transfers. The AP_0 provides the parity for address connections A_{23-3}, and AP_1 provides the parity for address connections A_{35-24}.

D. HIT#

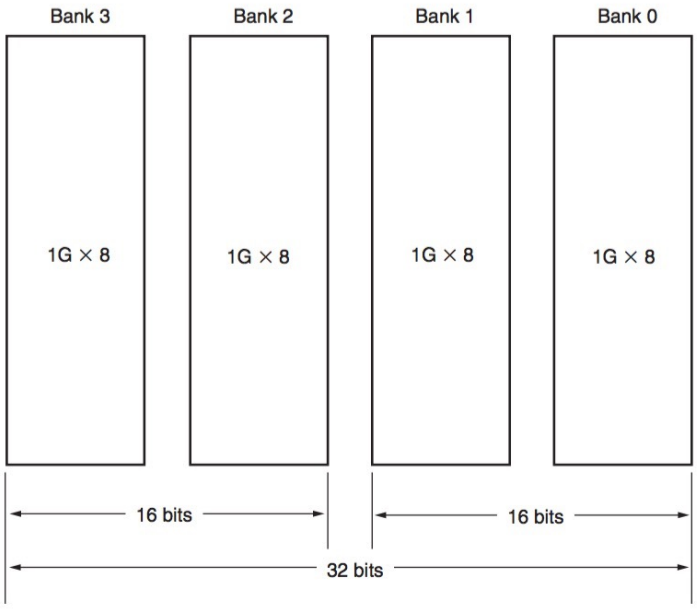
Hit shows that the internal cache contains valid data in the inquire mode.

E. HITM#

Hit modified shows that the inquire cycle found a modified cache line. his output is used to inhibit other master units from accessing data until the cache line is written to memory.

3.

A. Draw the memory system of 80386 and explain the same. Also write down the range of physical addresses for each of the memory banks and state the reason.



The physical memory system of the 80386 is 4GB in size and is addressed as such.

If virtual addressing is used, 64TB are mapped into the 4GB of physical space by the memory management unit and descriptors.

The memory is divided into four 8-bit wide memory banks, each containing

up to 1GB of memory. This 32-bit-wide memory organization allows bytes, words, or double-words of memory data to be accessed directly.

The 80386DX transfers up to a 32-bit-wide number in a single memory cycle.

The 80386DX uses a 32-bit-wide memory address, with memory bytes numbered from location 00000000H to FFFFFFFFH.

Memory location 00000000H is in bank 0, location 00000001H is in bank 1, location 00000002H is in bank 2, and location 00000003H is in bank 3, allowing 32 bits, (00000000H to 00000003H to be accessed at once).

Bank 0: 0000-0000H to FFFF-FFFCH
Bank 1: 0000-0001H to FFFF-FFFDH
Bank 2: 0000-0002H to FFFF-FFFEH
Bank 3: 0000-0003H to FFFF-FFFFH

B. In paging mode of 80386, a system is set up with one page directory. What should be the values of A_{22}-A_{31}, A_{12}-A_{21} so that 80386 selects the 901st page frame in 347th page table in the page directory? Show that the maximum memory for a page directory having base addresses of 1024 page tables is 4GB.

$A_{31\text{-}22} = 0101011011_2 = 347_{10}$
$A_{21\text{-}12} = 1110000101_2 = 901_{10}$

Page directory has 1024 pages.
Each page contains 1024 entries of 4KB each.
∴ Maximum memory of the page table directory = 1024 x 1024 x 4KB = 4GB

4.

A. Draw the block diagram of 80486.

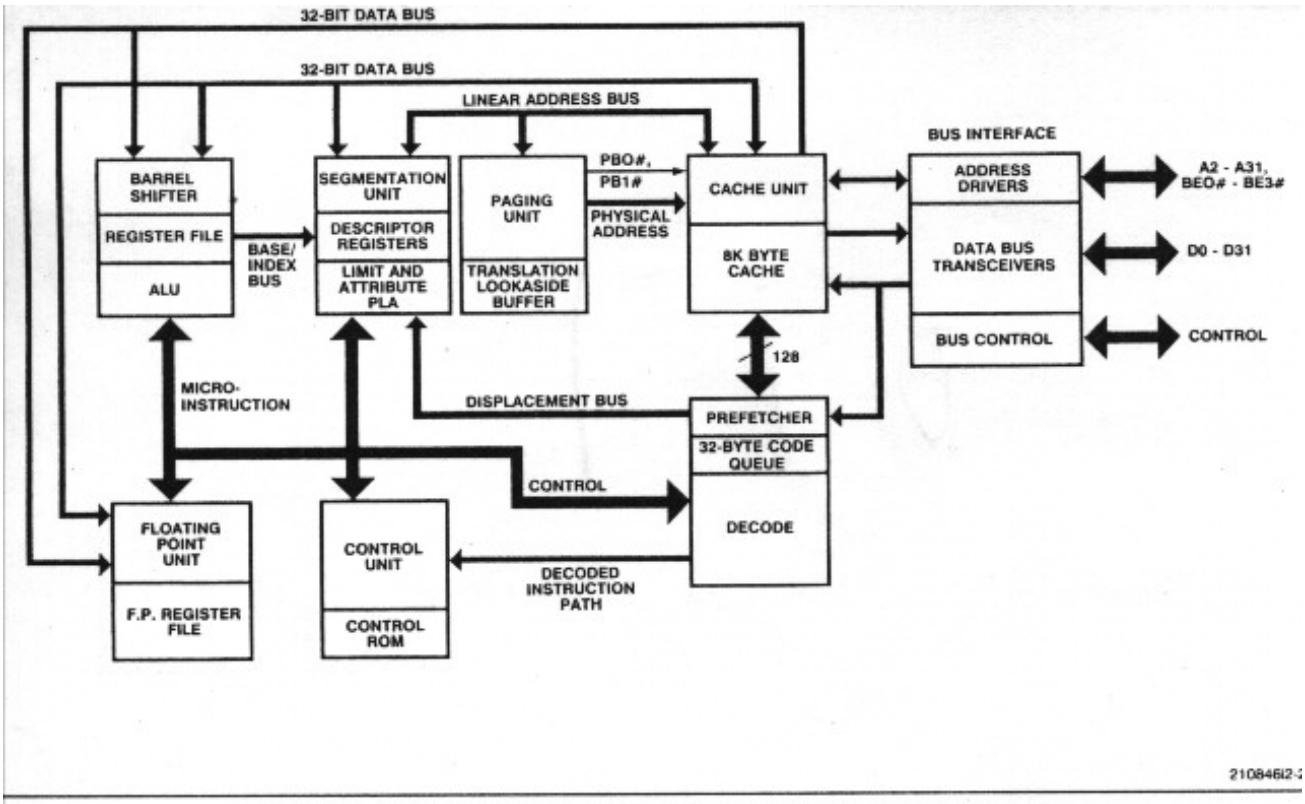


Figure 2-2. Intel486™ Microprocessor Pipelined 32-Bit Microarchitecture

B. Discuss the following signals of 80486:

A. DP_3 - DP_0

Data parity I/O provides even parity for a write operation and check parity for a read operation. If a parity error is detected during a read, the PCHK output becomes a logic 0 to indicate a parity error.

B. BUS SIZE 8

The **bus size 8** input causes the 80486 to structure itself with an 8-bit data bus to access byte-wide memory and I/O components.

C. CLK

The **clock** input provides the 80486 with its basic timing signal. The clock input is a TTL-compatible input that is 25 MHz to operate the 80486 at 25 MHz.

D. BE_{3-0}

Byte enable outputs select a bank of the memory system when information is transferred between the microprocessors and its memory and I/O space. BE_{3-0} selects D_{31-24}, D_{23-16}, D_{15-8}, D_{7-0}, respectively.

E. BRDY#

The **burst ready** input is used to signal the microprocessor that a burst cycle is complete.

F. FERR#

The **floating-point error** output indicates that the floating-point coprocessor has detected an error condition.

G. FLUSH#

The **cache flush** input forces the microprocessor to erase the contents of its 8K-byte internal cache.

H. IGGNE#

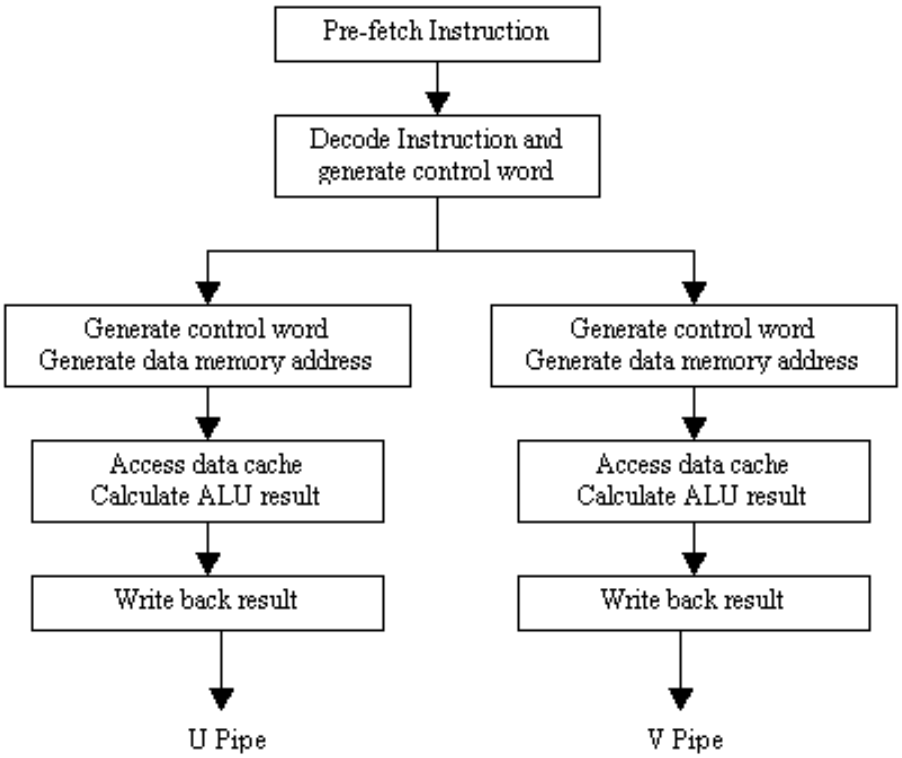
The **ignore numeric error** input causes the coprocessor to ignore floating- point errors and to continue processing data.

I. PCHK#

The **parity check** output indicates that a parity error was detected during a read operation on the DP_{3-0} bits.

5.

A. Explain the two integer pipelines of the Pentium processor with a neat diagram.



The two Integer pipelines in Pentium processor are labelled as U and V pipelines.

The V pipeline is for simple instructions, like addition and subtraction.
The U pipeline is for any instruction, like multiplication and division.

The two instructions proceed through the parallel pipelines at one stage per cycle, until they reach the register (result) write-back (WB) stage

B. Describe the 4 MB page and flat memory model in Pentium.

The paging mechanism functions with 4KB memory pages or with a new extension available to the Pentium with 4MB memory pages.

In the Pentium, the 4MB paging is dramatically reduced to just a single page directory and no page tables. The 4MB page sizes are selected by the PSE bit in control register 0.

The main difference between 4K paging and 4M paging is that in the 4M paging scheme there is no page table entry in the linear address.

A *flat mode memory* system is one in which there is no segmentation, i.e. memory appears to the program as a single contiguous address space. The CPU can directly (and linearly) address all of the available memory locations without having to resort to any sort of memory segmentation or paging schemes.

The Pentium microprocessor re-pages a linear address to a memory location in the 4MB pages, without employing any page table.