MP Assignment III

1. **An 8255A installed in a system has system base address E0D0H.**

   i) **Calculate the system addresses for the three ports and control register for this 8255A.**

   System base address = E0D0H = 1110 0000 1101 0000

   Port A address = E0D0H = 1110 0000 1101 0000
   Port B address = E0D1H = 1110 0000 1101 0001
   Port C address = E0D2H = 1110 0000 1101 0010
   Control word register address = E0D3H = 1110 0000 1101 0011

   ii) **Let's say the peripheral device is LED display and is connected to 8255A. Valid data is always available and I want it to be displayed on LED display all the time. Which type of parallel data transfer can be used for this purpose?**

   We use the simple I/O mode for LED display shit. The processor simply sends the data to output device and doesn't care about the data sent has been received or not by the device.

   8255 is driving a LED, connected to one of the output ports. It simply sends logic high to glow an LED. But it doesn't care about the signal reached to Led or not.

   Explain. Describe with an example how the ports of 8255A can be configured for this purpose.

   Configure 8255A in following I/O mode:
   PA — Output
   PB — Output
   PCU — Output
   PCL — Output

   The control word with I/O modes as mode '0' will be = $1\ 00\ 0\ 0\ 0\ 0\ 0_2 = 80H$.

   The control word will be outputted to control word register having add 03H. The relevant instruction will be follows:

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MOV DX, <#8 bit address#>
MOV AL, 80H
OUT DX, AL
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2.

i) Explain the pins that are specific to maximum mode of 8086.

In the maximum mode, the 8086 is operated by strapping the MN/MX pin to ground.

The pins that have a function in maximum mode are as given follows.

- **S_2, S_1 & S_0:-** The states bits indicate the function of current cycle. These signals are normally decoded by the 8288.

S_2	S_1	S_0	Function
0	0	0	INTR
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Op-code Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

- **LOCK: -** The LOCK output is used to look peripheral off the system. This pin is activated by using LOCK prefix on any instruction.
- **RQ/GT0 & RQ/GT1:-** The request/grant pins request DMA during the maximum mode operations of 8086. These lines are bi-directional and are used to request and grant a DMA operation.
- **QS1 & QS0:-** The queue states bit show the states of the internal instruction queue in 8086.

ii) Write short notes on Double handshake data transfer.

In *double handshake*, first the peripheral device sends a strobe signal, the microprocessor, sends the acknowledge signal to indicate that it is ready to receive data. After which data is received.After sending data, the peripheral sends a strobe signal to indicate data transmission completion, due to which, the microprocessor drops its acknowledge signal and a session has been completed.

3. In an environment there is only one 8259A. The mode is fixed priority mode.

There are three registers, an Interrupt Mask Register (IMR), an Interrupt Request Register (IRR), and an In-Service Register (ISR).

The IRR maintains a mask of the current interrupts that are pending acknowledgement.
The ISR maintains a mask of the interrupts that are pending an EOI.
The IMR maintains a mask of interrupts that should not be sent an acknowledgement.

i) IR5, IR3, IR1 are unmasked. Interrupt signal comes on IR5. Write down the sequence of actions with respect to the registers of 8259A.

Assuming IF = 1,

IR_5, IR_3, and IR_1 are lines raised high that set corresponding IRR bits.
All bits except the 1st, 3rd and 5th of the IMR are set.

When a signal comes on IR_5, the 5th bit in IRR is set. The *priority resolver sees that this bit is unmasked in IMR* and no other higher priority interrupts are being serviced from the ISR.

It activates the circuitry and sends an INT signal to 8086, The 8086 acknowledges with an INTA pulse.

Upon receiving an INTA signal from the CPU, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive data during this period.

The 8086 will initiate a second INTA pulse. During this period 8259A sends the interrupt type through a data bus to 8086.

The interrupt service routine starts execution by obtaining addresses from IVT and the 5th bit in the ISR is set.

ii) The first instruction in the ISR of interrupt on IR5 is STI. Execution now is in the middle of ISR of interrupt on IR5. Now an interrupt signal hits IR1. Write down the sequence of actions with respect to registers of 8259A.

When a signal comes on IR_1, 1st bit on the IRR is set. Priority resolver checks that this is unmasked, it also sees that a lower priority interrupt is being serviced.

Since 5th bit in ISR is set, it activates the circuitry and sends a high signal on INT pin to 8086, to which 8086 responds with an INTA.

8259A sends the vector type, it's address is obtained from the IVT and control goes to the respective ISPs. 1st bit in the ISR is now set.

iii) The first instruction in the ISR of interrupt on IR1 is STI. Execution now is in the middle of ISR of interrupt on IR1. Now an interrupt signal hits IR6. Write down the sequence of actions with respect to registers of 8259A.

When a signal comes on IR_6, 6th bit on the IRR is set. Priority resolver checks that this bit in IMR is masked. Thus no action is taken.

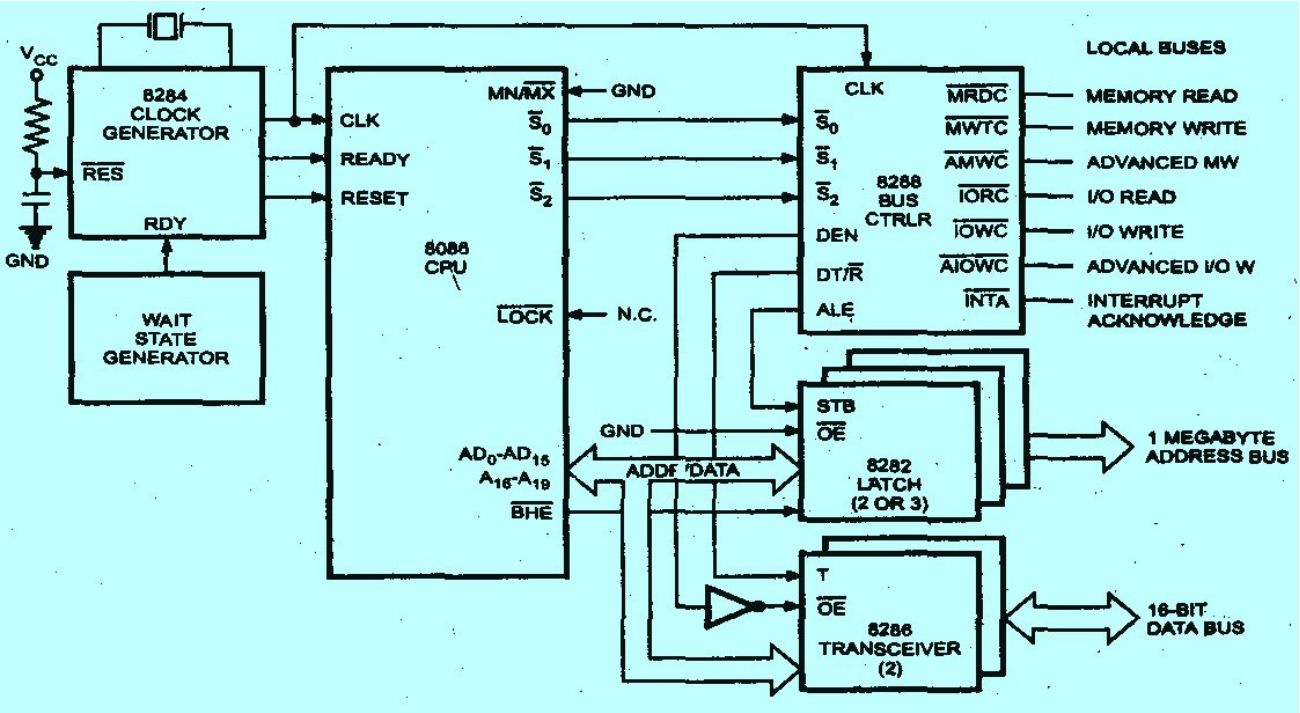
The ISP of the interrupt being executed, IR_1 continues. A control word is sent to 8259A to reset 1st bit in the ISR, so that lower priority interrupts can be executed.

When IRET instruction of IR_1 is executed the control returns to the ISP of IR_6, and when that ends, the control reaches the main program.

(Thanks Shamathmika for the answer)

4.

i) Draw the maximum mode system diagram.



ii) What would be the control word if I want counter 2 of 8254 to be BCD down counter, to generate rectangular wave, read/write most significant byte only?

$$1\ 0\ 1\ 0\ 0\ 1\ 1\ 1 = A7_H$$

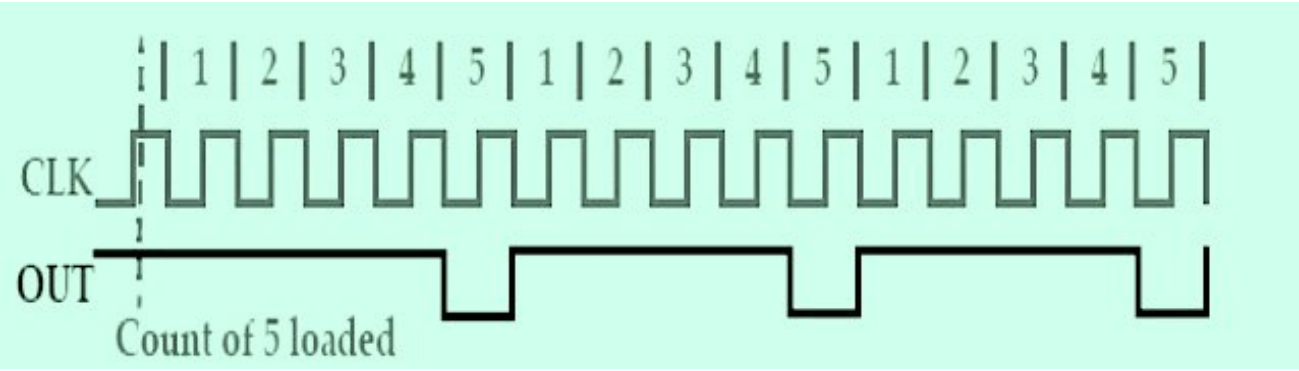
5.

i) Draw an example waveform to describe mode 2 of 8254.

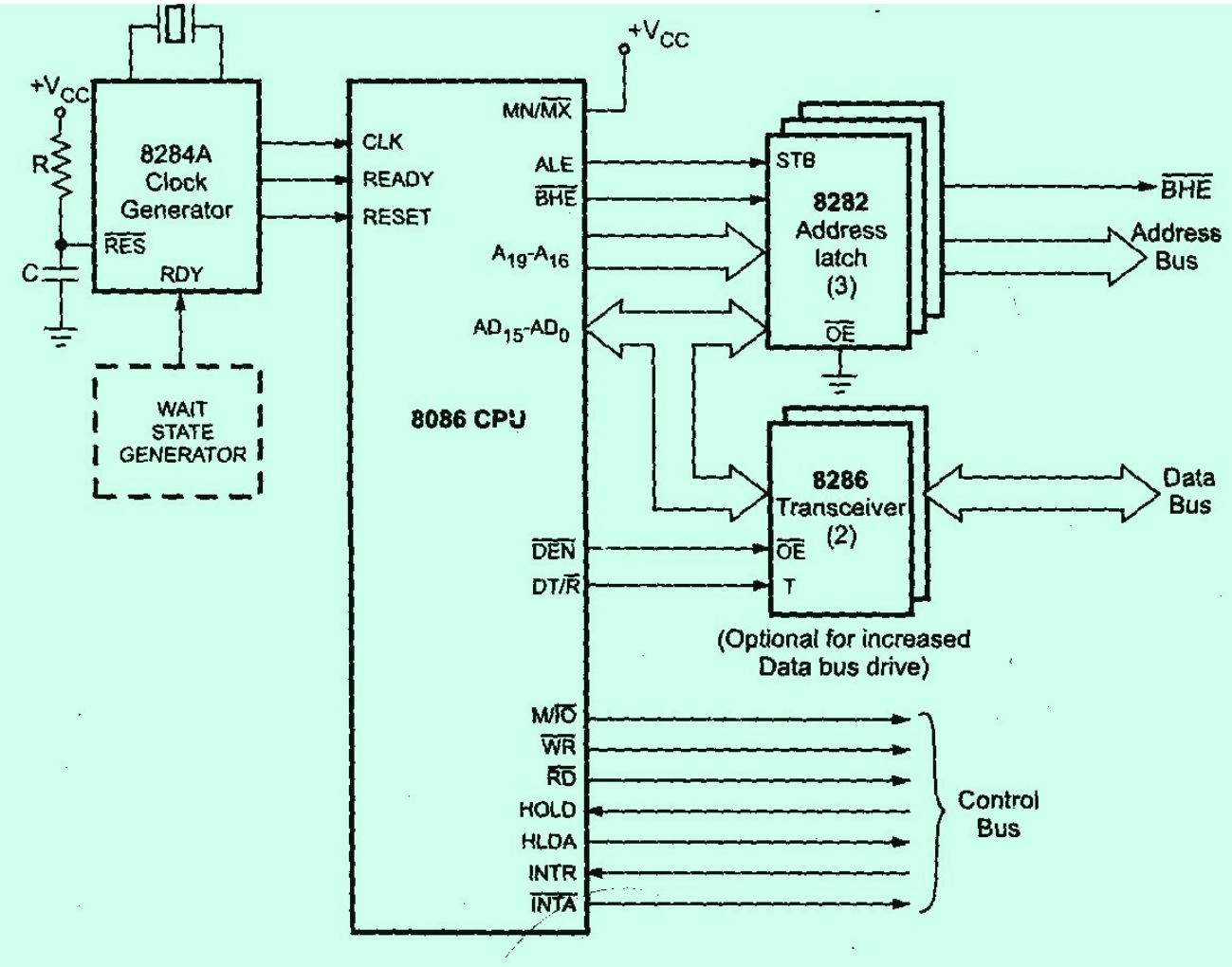
Mode 2 - Rate generator / Divide by N counter.

- After N pulses, OUT goes low for only one clock cycle.
- Then count is reloaded, and out stays high for N clock cycles.

The number of clock cycles between two low pulses = the count loaded.



ii) Draw the minimum mode system diagram.



Here's some potatoes.